

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (original): A semiconductor package comprising:
  - a die having a plurality of layers of low-K dielectric material, the die having a top surface, a bottom surface, and a plurality of side surfaces, each surface having associated corner and edge regions;
  - a wire bonding packaging substrate having a plurality of electrical contacts, the packaging substrate being positioned under the die;
  - a plurality of interconnects electrically connecting the die to the plurality of electrical contacts;
  - a molding interface material applied to at least a portion of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die; and
  - a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material.
2. (currently amended): A semiconductor package as recited in claim 1, wherein the molding interface material is configured to introduce controls by applying compressive stress to the die, ~~thereby~~ and strengthening the die against the at least one of tensile and shear stresses.
3. (original): A semiconductor package as recited in claim 1, wherein the molding interface material is polyimide.
4. (original): A semiconductor package as recited in claim 3, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die.
5. (currently amended): A semiconductor package as recited in claim 4, wherein the molding interface material is also on a corresponding adjacent portion of the packaging substrate in order to secure such that the die is firmly attached to the packaging substrate.

6. (currently amended): A semiconductor package as recited in claim 1, wherein the molding interface material covers ~~is applied in~~ multiple non-contiguous regions on ~~to~~ the top surface of the die.

7. (original): A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape.

8. (original): A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape.

9. (original): A semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns.

10. (original): A semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the top surface of the die excluding corner regions.

11. (original): A semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns.

12. (original): A semiconductor package as recited in claim 10, wherein the molding interface material is a contiguous region on the top surface of the die excluding edge regions.

13. (original): A semiconductor package as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns.

14. (original): A semiconductor package as recited in claim 1, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm.

15. (original): A semiconductor package as recited in claim 14, wherein the molding interface material is over a substantial portion of the die such that a stress buffer zone is established between the die and the molding cap.

16. (original): A semiconductor package as recited in claim 1, wherein the plurality of layers includes extra low-K dielectric material.

17-36. (canceled)

37. (new): A semiconductor package as recited in claim 1, wherein the molding interface material is a layer positioned between and in contact with the die and the molding cap.

38. (new): A semiconductor package as recited in claim 1, wherein the plurality of low-K dielectric material has a CTE between the range of 20 ppm and 50 ppm.

39. (new): A semiconductor package as recited in claim 38, wherein the plurality of low-K dielectric material has a dielectric constant between 2.6 and 3.5.

40. (new): A semiconductor package as recited in claim 38, wherein the plurality of low-K dielectric material has a dielectric constant between 2.2 and 2.6.